Claims

1. A control unit (RE) having at least one control element (FA1...FA8), in particular having at least one integrating transfer characteristic (FA6, FA8) and/or differentiating transfer characteristic (FA7),

characterized in that

the control element (FA1...FA8) is constructed as a temporally discrete dynamic fuzzy logic control element (FAx), which has a memory device (MZ) for buffer storage of a current internal state variable (Z(i)) on the basis of fuzzy logic conclusions (F1, I1, D1, F2, I2, D2).

2. The control unit (RE) of claim 1,

characterized in that

the fuzzy logic control element (FAx, FA1...FA8), from an input variable (e(i)) and from an internal state variable (z(i)) on the basis of fuzzy logic conclusions (F1, I1, D1, F2, I2, D2) updates (z(i+1), f(z(i), e(i))) the internal state variable (z(i)) and generates (G(Z(i), e(i))), an output variable (y(i)) in such a way that the fuzzy logic control element (FAx) has at least one integrating and/or differentiating, in particular nonlinear transfer characteristic (e(i), y(i)) (Fig. 7a).

3. The control unit (RE) of one of claims 1 or 2,

characterized in that

the fuzzy logic control element (FAx) has at least one first static fuzzy logic device (F(z(i), e(i))) for updating the internal state variable (z(i)) of the fuzzy logic control element (FAx) on the basis of fuzzy logic conclusions (Fig. 7b).

4. The control unit (RE) of one of claims 1 through 3,

characterized in that

the fuzzy logic control element (FAx) has at least one second static fuzzy logic device (G(z(i), e(i))) for updating the output variable (y(i)) of the fuzzy logic control element (FAx) on the basis of fuzzy logic conclusions (Fig. 7c).

5. The control unit (RE) of one of claims 1 through 4,

characterized in that

a) the internal state variable (z(i)) of the fuzzy logic control element (FAx) is formed by at least one succession of processing states (Zm'...Z1', Z0, Z1..Zn), and

b) the fuzzy logic control element (FAx), upon an updating of the internal state variable (z(i)) from a previous processing state (Zm'...Zn) changes over in temporally discrete fashion into a subsequent processing state (Zm'...Zn) (Fig. 8, Fig. 9).

6. The use of a control unit (RE) of one of the foregoing claims for regulating a technical process.